Amendments to the Specification

Please amend the following paragraphs of the specification as originally filed:

[0006] One or more input devices are coupled, directly or indirectly, to each of the input processors. Each input device provides one or more input signals to the input processors. One or more output devices are coupled to the output processors. Each output device receives an output signal from an output ~~device~~processor. Each of the input processors generates one or more packetized signals. Each packetized signal is transported across a communications link to one or more of the output processors. Each output processor may receive one or more packetized signals.

[0026] The input signals 110 may be base-band, compressed, time division multiplexed audio signals, video signals (which may also include audio information), metadata, or other data signals. Similarly, the output signals 114 may be audio signals, video signals, or data signals. Typically, each output signal 114 will correspond to one or more of the input signals and or information derived from the input signal. A particular output signal may include a combination of audio, video or data input signals or signals produced by input signal analyzers or any combination of these types of signals. The nature of each output signal 114 is appropriate for the output device 116 that receives the output signal 114. Some of the output devices 116 may be video monitors, such as analog video monitor 116a and digital video monitor 116b, for displaying output video signals. Some of the output devices 116 may be sound systems, such as sound amplification and broadcast system 116c, for further processing or playing output audio signals. Some of the output devices may be data processing systems, such as computer system 116d, for further processing or displaying the output data signals. In any particular embodiment of the present invention, the output signals ~~116~~114 may be of the same or different types, depending on the usage of the embodiment. In an alternative embodiment of the invention, the

output processor may provide only a single output signal. The type of any particular signal may change depending on the usage of the signal, under the control of the master controller 102.

[0028] Memory system 122 may be a local memory device or memory space within the input processor 104 or it may be located on an attached storage device or other medium. Data buffers 124 will typically comprise memory space allocated within memory system ~~120~~122.

[0038] In the present embodiment, the signal processors 126 include video scalers 160, embedded audio extractors, ancillary data extractors, signal content analysers ~~160~~ and data compressors 164. The signal processors 126 may also include data de-compressors, image rotation devices, special effects processors, image invertors, spatial filters, edge enhancement processors, color space converters, audio sweetening processors, digital audio decompressors, and digital audio processors. A signal processor may be used to process two or more input signals (or processed signals) by time-division-multiplexing the signal processor between the data buffers used to buffer the two or more input signal (or processed signals).

[0039] Each video input signal 110 will have height and width dimensions, usually defined in pixels. For example, a video image may comprise a series of frames that are 640 pixels wide by 400 pixels high. A video scaler 160 is capable of rescaling a video signal from its original dimensions to different dimensions. In the present embodiment, the input processor 104 includes a plurality or bank of video scalers 160. Each video scaler 160 receives control instructions from the input processor local controller 140 to extract a particular video input signal 110 from the appropriate data buffer 124 and rescale the video input ~~scale~~signal to specified dimensions and to store the resulting processed signal 158 in another data buffer 124. A video scaler 160 may be configured to retain or change the aspect ratio of an input data signal or to crop the input data

signal in the processed signal and to provide any other function that a conventional scaler is capable of providing. For example, a video scaler may be configured to crop the input data signal to select a portion of it, and then scale the cropped video image to specified dimensions.

[0042] The data compressors 164 may include horizontal or vertical line filters that produce a processed video data signal comprising a portion of the video data from a video input data signal. For example, a horizontal line filter may be configured to horizontally compress a 640 x 400 pixel video signal into a 320 x 400 pixel video signal by discarding every other pixel in each line of the video signal. A vertical line filter may be configured to compress a 640 x 400 pixel video signal into a ~~320~~640 x ~~400~~200 pixel video signal by discarding every other line in the video signal. A horizontal/vertical line filter may be configured to compress a 640 x 400 video signal into a 160 x 100 video signal by discarding three of every four lines of the video signal and discarding three of every four pixels in each line that is retained.

[0046] To further explain the invention and the present embodiment, an example of the use of this embodiment will be described. In the example, the input processor 104 receives three digital video input signals 110a, 110b and 110d and one analog video input signal 110e. Analog video input signal 110e is digitized using a A/D converter 150 to produce a digital signal 110e' corresponding to analog signal 110e. Signals 110a, 110b, ~~110e~~110d and 110e' are buffered in separate data buffers 124.

[0047] Reference is made to Figure 3, which illustrates output device 116a, which is an analog standard definition 4:3 format video monitor capable of displaying images with a resolution of 640 x 480 pixels. The display of video monitor 116a is used to display information in five different parts or windows: video windows 170, 172, 174 and ~~175~~176 and graphics window 178.

[0051] The video windows have been described as containing "a version of" one of the video input signals 110. The user will typically specify the position and dimension of a window on a video monitor and the input signal 110 that the user would like displayed in each window. An appropriate version of the input signal is prepared by the input processor 104 and provided to the output processor ~~104~~106 for display on the video monitor. Alternatively, the user may specify certain signal processing steps to be performed on an input signal before it is displayed in a window. For example, if the signal processors 126 (Figure 2) include a color / black & white converter, then a user may specify that a color input signal be converted into a black & white signal and that the black & white version of the input signal (or a version of the black & white signal) be displayed in a particular window.

[0052] Reference is again made to Figure 1. The user controller ~~106~~118 transmits the user's instructions for each output device 116 to the master controller as user control signals 119. The user's instructions relating each output device 116 will typically depend on the nature of the output device 116. For example, if an output device 116 is an audio processing system capable of receiving and switching between multiple audio signals, then the user may specify that one or more audio input signals 110, or the audio components of video input signals 110, be directed to the sound output device 116. If an output device 116 is only capable of receiving a single audio signal and then amplifying and broadcasting the audio signal, the user may specify that a particular input audio signal or the audio component of a particular video input signal 110 be directed to the sound output device 116. Similarly, a user may specify that any particular output device 116 can receive any combination of information that the output device is capable of receiving.

[0057] In response to the input processor control signals 120, the input processor local controller 140 determines how the required ~~the~~ versions of each input signal 110 can be produced and configures and couples the input ports 123, A/D converters 150,

data buffers 124 and signal processors 126 to produce the required versions of each input signal. As described above, every signal stored in a data buffer 124 is assigned a unique global identification code.

[0058] In the present example, the input processor local controller 140 configures the input processor 104 as follows:

i. Store input signal 110a in data buffer 124a. Assign global identification code G101 to the stored signal.

ii. Store input signal 110b in data buffer 124b. Assign global identification code G102 to the stored signal.

iii. Store input signal 110d in data buffer 124c. Assign global identification code G103 to the stored signal.

iv. Couple an A/D converter 150 between input port 108e at which input signal 110e is received to produce a digital version 110e' of input signal 110e. Store digital signal 110e' in data buffer 124e. Assign global identification code G104 to the stored signal.

v. Couple video scaler 160a to memory system 122 to retrieve signal G101 and produce a scaled version of 400 x 300 pixel scaled version of signal G101. The scaled version is stored in data buffer 124f and is assigned global identification code G105.

vi. Couple video scaler 160b to memory system 122 to retrieve signal G101 and produce a 610 x 460 pixel scaled version of signal G101. The scaled version is stored in data buffer 124g and is assigned global identification code G106.

vii. Couple video scaler 160c to memory system 122 to retrieve signal G102 and produce a 200 x 113 pixel scaled version of signal G102. The scaled version is stored in a memory buffer 124h and is assigned global identification code G107.

viii. Couple video scaler 160d to memory system 122 to retrieve signal G102 and produce an 1140 x 640 pixel scaled version of signal G102. The scaled version is stored in data buffer 124i and is assigned global identification code G108.

ix. Couple video scaler 160e to memory system 122 to retrieve signal G103 and produce a 160 x 120 pixel scaled version of signal G103. The scaled version is stored in data buffer 124j and is assigned global identification code G109.

x. Couple video scaler 160[[e]]f to memory system 122 to retrieve signal G104 and produce a 560 x 420 pixel scaled version of signal G104. The scaled version is stored in data buffer 124k and is assigned global identification code G110.

xi. Couple a signal analyzer (one of the signal processors 126, as described above) to the memory system 122 to retrieve and analyze signal G102. The signal analyzer produces a video signal with a standard size of 320 x 200 pixels and metadata. The output of the signal analyzer is stored in data buffer 124m and is assigned global identification code G111.

xii. Couple a video scaler 160[[f]]g to memory system 122 to retrieve signal G111 and produce a 440 x 140 pixel scaled version of signal G111. The scaled version is stored in data buffer 124n and is assigned global identification code G112.

[0061] Reference is next made to Figure 5, which illustrates the format of the packetized signal 112. In the present embodiment, the packetized signal 112 comprises a series of packets 190, each of which contains the following fields:

i. global identification code for the signal from which the data in the packet was obtained;

ii. packet ordering information;

iii. a data payload;

iv. optional error detection and correction information and other metadata.

[0065] For example, if a packet source signal comprises a stream of data that is not organized as packets of information, then each packet 190 formed from that packet source signal contains a fixed amount of data in the data payload field. For example, if a packet source signal is a continuous stream of video data, then each corresponding packet 190 contains up to 320 bytes of the video data. In other embodiments, the amount of data in a particular packet may be fixed at a different size or may be variable.

[0070] The last packet 190 used to packetize each frame of video signal G107 contains data for only 200 pixels. The remaining data space is filled with [[N]]null characters by the packetized signal formatter 128. Alternatively, the last packet may have a shortened data payload length.

[0075] Reference is made to Figure 1. In the present embodiment, the packetized signal output port ~~112~~138 will typically be coupled to the output processor (Figure 1) through a communication link 186, which may be a data cable such as an electrical or optical cable. The data rate and other aspects of the data protocol used to transmit the packetized signal 112 correspond to the ability of the communication link 186.

[0076] In other alternative embodiments, the packetized signal generator ~~128~~132 may transmit the buffered packets 190 as an asynchronous stream of packets to the output processor using any communication protocol, including TCP/IP. In this case, the communication link 186 may be a cable or may be a LAN, WAN, the Internet or another communication system.

[0077] Reference is next made to Figure 6, which illustrates the output processor 106. The output processor 106 has a packetized signal input port 202, a packetized signal input stage 205, a memory system 208, a plurality of signal processor 210, an output signal generator 212, a bank 213 of digital-to-analog (D/A) converters 215, a plurality of output ports 214 and one or more local signal generators 224. Each packetized signal input stage 205 comprises a packetized signal input buffer 204, a packetized signal extractor 206. The display devices 116 are coupled to the output ports ~~210~~214. The output processor 106 also includes an output processor local controller 216 that receives output processor control signals 121 from the master controller 102 (Figure 1). The output processor local controller 216 is coupled to the various components of the output controller 106 through control lines 218 and controls the operation of those components in response to the output processor control signals 121.

[0081] The packetized signal 112 is received at input port 202 and is buffered in packetized stream input buffer 204. As complete packets 190 are stored in buffer 204, ~~there~~they are retrieved by packetized signal extractor 206. The packetized signal extractor 206 determines the global identification code of each packet, translates the global identification code into the corresponding local identification code assigned by output processor local controller and stores packets 190 corresponding to each local identification code in a different data buffer 220. Through this process, the data from each source signal for the packetized signal is isolated in a different data buffer 220. Each isolated signal corresponds to one of the packet source signals for the packetized signal. The packet ordering information from each packet 190 is used to organize the packets 190 into their original sequence. Each isolated signal is referred to herein as an output source signal.

[0083] The signal processors 210 may be used to reverse any compression or other signal processing operation applied in the input processor 104 (Figure 2) using the

signal processors 126. Depending on the signal processing operations performed in the input processor ~~106~~104, a reversing step may or may not be required. For example, if one of the input signals 110 was compressed using a standard compression format that may be directly used to produce an output signal 114, then it is not necessary to reverse the compression. However, if the result of the compression step produced data that cannot be directly used to produce an output signal 114, then a decompressor may be used to reverse the compression step. For example, one of the signal processor described above was a horizontal line filter, which compresses an input video signal 110 by discarding a portion of the video signal. This compression step may be reversed by interpolating the discarded data from the retained data. The resulting processed signal 222 is stored in a data buffer as an output source signal and is assigned a unique local identification code by the output processor local controller 216.

[0086] The output signal generator 212 can generate a variety of digital output signals that may be used directly, or after conversion through a D/A converter 215, by output device 116. The output signal generator 212 may include one or more digital video signal generators, one or more digital audio signal generators or one or more data signal generators or any combination of video, audio and data signal generators. The data signal generators may include TCP/IP signal generators that produce an output signal 114 suitable for transmission using a communications link to a remote computer system, where the output signal may be decoded and used by a video, audio or data system. Similarly, the data signal ~~generators~~generate may generator signals in any data format.

[0090] To produce the video signals for the example output video monitors 116a (Figure 3) and 116b (Figure 4), the output processor local controller configures the output ~~controller~~processor 106 to operate as follows:

i. Packetized signal extractor 206 operates as follows:

   a. Extract signal G105 from the packetized signal 112 stored in packetized stream input buffer 204, assign it local identification

code B201 and store it as an output source signal in data buffer 220a;

b. Extract signal G106 from the packetized signal 112 stored in packetized stream input buffer 204, assign it local identification code B202 and store it as an output source signal in data buffer 220b;

c. Extract signal G107 from the packetized signal 112 stored in packetized stream input buffer 204, assign it local identification code B203 and store it as an output source signal in data buffer 220c;

d. Extract signal G108 from the packetized signal 112 stored in packetized stream input buffer 204, assign it local identification code B204 and store it as an output source signal in data buffer 220d;

e. Extract signal G109 from the packetized signal 112 stored in packetized stream input buffer 204, assign it local identification code B205 and store it as an output source signal in data buffer 220e;

f. Extract signal G110 from the packetized signal 112 stored in packetized stream input buffer 204, assign it local identification code B206 and store it as an output source signal in data buffer 220f; and

g. Extract signal G112 from the packetized signal 112 stored in packetized stream input buffer 204, assign it local identification code B207 and store it as an output source signal in data buffer 220g.

ii. Local signal generator 224 produces a 200 x 150 pixel data and time window as described above. Assign local identification code B208 to this signal and store it as an output source signal in data buffer 220h.

iii. Output signal generator 212 generates two output signals as follows:

a. One output video signal generator 212a extracts local signals B201, B203, B205, B207 and B208 from the corresponding data buffers 220 and produces an output signal 114a.

b. A second output video signal generator 212b extracts local signals B202 B204 and B206 from the corresponding data buffers 220 and produces an output signal 114b.

iv. A D/A converter is coupled between video signal generator 212a and output terminal to convert output signal 114a into a digital output signal, which is then displayed by video monitor 116a.

v. Output signal 114b is coupled directly to output port 214b. Video monitor 116b receives and displays the digital output signal 114b.

[0091] Referring to Figure 1, the input processor ~~102~~104 receives a plurality of different input signals 110, which are asynchronous with respect to one another to be received at the input processor. The input signals are processed using signal processor 126 to put them into a format that is required for the output signals 114 and resulting processed signal (the packet source signals) are combined into a single packetized signal 112. If an input signal 110 does not require any processing to be used as part of an output signal, the ~~output~~input signal 110 may be a packet source signal. The input processor allows a plurality of asynchronous data signals 110, which may include video, audio and data signals, to be combined into a single packetized signal that may be transmitted using a single communication link 186.

[0094] In the embodiment of Figures 1 to 6, the input processor 104 includes video scalers 160 to scale video input signals 110 from their original dimension to other dimensions required for the output signals 114. In some cases, this may required that the input video signal may be expanded to large dimensions, resulting in a packet source signal that requires a larger portion of the packetized signal bandwidth to

transmit than the original input signal 110. To reduce this increased usage of bandwidth, another embodiment of the invention may be configured to ensure that the scalers 160 in the input processor 104 are only used to reduce an input signal ~~160~~110 to smaller dimensions. Video scalers may be included in the output processor as signal processors ~~220~~210 to scale any input signal that must be enlarged before it is incorporated into an output signal.

[0095] Reference is next made to Figure 7, which illustrates a second input processor 304. Input processor 304 is similar to input processor 104 (Figure 2) and similar components are given similar reference numbers. The input processor local controller 340 is coupled to the various components of the input processor 304. These couplings are not illustrated to simplify the Figure. Input processor 304 has a plurality of packetized signal output stages 327, each of which comprises a packetized signal formatter 328, packetized signal buffer 330 and packetized signal generator 332. Each packetized signal output stage 327 is capable of generating a packetized signal 112. Each packetized signal 112 may include information of any one or more of the input signals 110. Input processor 304 may be used to provide packetized signals to different output processors 106 (Figure 7). Each output processor can receive a packetized signal containing only information from packet source signals that are required to produce the output signals 114 produced by that specific output processor.

[0097] Reference is next made to Figure 8, which illustrates a second output processor 403. Output processor 403 is similar to output processor ~~104~~106 (Figure 6) and similar components are identified with similar reference numbers. ~~Input~~Output processor 403 has a plurality of packetized signal input stages 405, each of which comprises a packetized signal input buffer 404 and a packetized signal extractor 406. Each input stage 405 receives a packetized signal 112 at a packetized signal input port 202 and stores the data for each source signal for each packetized signal in a separate data buffer in memory system 208. This allows output processor 403 to receive a larger

number of source signal than could be transmitted in a single packetized signal. Output processor 403 operates in the same manner to further process and generate output signals 114, which may incorporate data from one or both of the packetized signals.

[0098] Reference is next made to Figure 9, which illustrates three input processors 304 and two output processors ~~306~~403. Input processor 304a receives eight input signals from eight sources 108a – 108h and generates two packetized signals 112a and 112b. Input processor 304b receives eight input signals from eight sources 108i – 108p and generates two packetized signals 112c and 112d. Input processor 304c receives eight input signals 108q – 108x and generates one packetized signal 112e. Output processor 403a receive packetized signals 112a and 112c and produces four output signals 114a – 114d at output terminals ~~214a~~714a – ~~214d~~714d. These output signals may include information from any of the sixteen input signals 108a – 108p. Output processor 403b receives packetized signals 112b, 112d and 112e and produces four output signals 114e – 114h at terminals ~~214e~~714e – ~~214h~~714h. The output signals 114a – 114h may include information from any of the twenty-four input signals 108a – 108x. In each case, each input source is coupled to only one input ~~terminal~~processor, but may be combined with the other input sources in the output signals.

[00102] Each packetized signal output stage 527 operates independently of the others. Any number of packetized signals 512 generated by the packetized signal output stages may include packets from the same data buffer 510 (corresponding to a particular global identification code). Each data buffer is operated to ensure that each packet in the data buffer are not discarded until each ~~the~~ packet has been read by every packetized signal output stage that requires the packet.

[00104] Inserting packet router 502 between a plurality of input processors 104 and 304 and output processors ~~104~~106 and 403 allows an input signal 110 received at

any one of the input processors to be routed (possibly after being processed in the input processor by signal processor 126) to any of the output processors for use by any of the output devices 116 coupled to an output processor. Each input signal is received in only one location, but may be used in multiple formats (by creating appropriate versions of the input signal using signal processor 126) at multiple output devices 116.

[00107] The packet router controller 604 receives router control instructions 620 (similar to the router control instructions 520 received by packet router controller 502 (Figure 10)) from master controller 102 instructing the packet router controller to generate the packetized links 612 using packets 190 with specified global identification codes. The packet router controller 604 determines and assigns one of the packetized signal output stages ~~527~~627 to generate each of the required packetized signals 612 and maintains a global identification code distribution table 613 correlating each global identification code with the packetized signal output stages 627 that require the global identification code. For example, a specified global identification code G603 may be required for three of the outgoing packetized signals 612. The three packetized signal output stage 627 used to generate those three packetized signals 612 are listed in the global identification code distribution table 613 in association with global identification code G603.

[00110] For example, each packet 190 with global identification code G603 may be required by packetized signal output stages 627a, 627c and 627d to produce outgoing packetized signal 612a, 612c and 612d. When a complete packet 190 with global identification code G603 is received, router controller 604 selects a free packet storage location 610b and instructs the appropriate packetized signal extractor ~~508~~608 to store the packet 190 in packet storage location 610b. The router controller 604 then sets the status of packet storage location 610b to "3", indicating that the packet 190 must still be read by three packetized signal output stages. The router controller than instructs packetized signal output stages 627a, 627c and 627d to read the packet 190.

Each of packet selectors 628a, 628c and 628d reads the packet 190 and indicates to router controller 604 that it has done so. Router controller 604 decrements the status of the packet storage location 610b as it receives each indication and when the status returns to "0", the packet storage location 610b is again free to store another packet 190.

[00111] Reference is next made to Figure 12, which illustrates a third packet router 702. Packet router 702 is similar in structure and operation to packet router 602 and similar components are identified with similar reference numbers, increase by one hundred. Packet router 702 has a plurality of signals processors 726 coupled to memory system 709. Signal processor 726 operate in a similar manner to signal processors 210 (Figure 6) under the control of router controller 704. Router controller 704 receives instructions from master controller 102 to perform one or more signal processing steps on the signal encoded with a particular global identification code. For example, the master controller may indicate that a video signal with global identification code G734 must be scaled to dimensions of 800 x 600 pixels and the resulting processed signal is to be assigned global identification code G783 and must be included in packetized signals 712b and 712c. Router controller 704 then configures the global identification code distribution table 713 to route packets with global identification code G734 to a video scaler ~~760~~(not shown) among the signal processors 726. The router controller 704 may also route the same packet to one or more other signal processors 726 or packetized signal output stages 727. The video scaler ~~760~~(not shown) is configured to perform the video scaling operation and produces packets 190 identified with global identification code G783. These packets are stored in free packet storage locations as designated by the router controller 702. The packets are then distributed to packetized signal output stages 727b and 727c using global identification code distribution table 713 and storage location table 711.

[00112] Reference is next made to Figure 13, which illustrates an output stage 827 for an output processor. Output stage 827 may be used for video output signals and includes a buffer 840 coupled to output signal generator 212 and an output terminal ~~842~~214. The output signal 114 generated by the output signal generator 212 is stored in data buffer 840. The stored signal is extracted from the data buffer 840 by a local output generator ~~832~~842 which makes the output signal 114 available at an output terminal 214. Optionally a D/A converter may be coupled between the local output generator 842 and output terminal 214 to convert the output signal into a corresponding analog output signal for use by an analog device coupled to terminal 214.

[00117] Reference is next made to Figure 14, which illustrates a switch 860 coupled between a plurality of graphics packet signal ports 848, which may be part of one or more output stage 827 in one or more output processors, and a plurality of display interfaces 852. The switch 860 may be implemented as a physical switch, which may be manually operable or automatically operable under the control of the master controller 102 (not shown in Figure 12). The switch 860 may be implemented using a field-programmable gate array (FPGA) or with any other switching or packet routing technology. Switch 860 allows any of the graphics packet signal ports 848 to be coupled to any display interface 852, allows any of the ~~input~~output signals 114 available at any of the graphics packet signal ports 848 to be displayed at any display monitor coupled to a display adapter 852.